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# PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
**ST-99-AD-037**

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on_____

Signature_____

Typed or printed name_____

| Application Number | Filed |
|---|---|
| **10/016,972** | **12/14/2001** |

First Named Inventor
**Allen**

| Art Unit | Examiner |
|---|---|
| **2188** | **Mardochee Chery** |

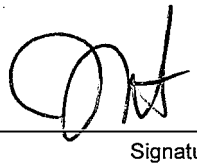
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheets.
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 35,272
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____



Signature

Ira S. Matsil
Typed or printed name

972-732-1001
Telephone number

6/5/08
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Applicant: | Allen | Docket No.: | ST-99-AD-037 |
| Serial No.: | 10/016,972 | Art Unit: | 2188 |
| Filed: | December 14, 2001 | Examiner: | Chery, Mardochee |
| For: | Disk Controller Providing for the Auto-Transfer of Host-Requested-Data From a Cache Memory Within a Disk Memory System | | |

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Dear Sir:

Applicants appeal the final rejection of all pending claims 1-9 and 27-30, which were rejected as being unpatentable over U.S. Patent 5,696,931 (hereinafter "Lum") over U.S. Patent 6,141,728 (hereinafter "Simionescu"). Applicants respectfully submit that the claims of the present application are patentably different from Lum over Simionescu.

*Summary of Arguments*

1. The presently presented claims relate to a system that provides for (1) transferring requested data from a cache to a host, (2) transferring (other) requested data from a mass storage device directly to the host, and (3) steps (1) and (2) occur substantially concurrently.

2. Examiner concedes that Lum does not teach transferring a portion of requested data from cache to host system substantially concurrently with transferring a portion of requested data from a mass storage device to the host.

3. Simionescu merely teaches (1) transferring requested data from a cache to a host, (2) transferring (other) requested data from a mass storage device to the cache, and (3) subsequently transferring the (other) requested data from the cache to the host.

4. Transferring data from a mass storage device to a cache and subsequently transferring the data to the host is not transferring "directly to the host system."

5. Transferring data from a cache to a host concurrently with transferring (other) data from a mass storage device directly to the host is not the same as transferring data from a cache to a host concurrently with transferring data from mass storage to the cache.

*Discussion*

Exemplary claim 1 recites a system comprising a mass storage device, a cache memory coupled to the mass storage device, a microprocessor coupled to the mass storage device and the cache memory, and a controller coupled to microprocessor and the cache memory. Under appropriate circumstances, the controller "initiates an auto-transfer of . . . data that resides in the cache to the host system; and requests a transfer of . . . data that resides in the mass storage device directly to the host system, wherein the request of the transfer and the initiation of the auto-transfer occurs substantially concurrently" (emphasis added). Simply, the cited claim element requires (1) transferring requested data from the cache to the host, (2) transferring requested data from mass storage directly to the host, and (3) steps (1) and (2) occur substantially concurrently.

Examiner concedes that Lum does not teach transferring a portion of requested data from cache to host system substantially concurrently with transferring a portion of requested data from a mass storage device to the host (Final Rejection, 04/20/2008).

To overcome the conceded shortcoming of Lum, Examiner relies upon Simionescu, to wit: "This process of rescanning and transferring continues until the transfer of all of the

requested sectors (*requested data*) is completed. At the same time, firmware causes the disk drive to read additional sectors from disk into the cache buffer, and these additional sectors are located during rescanning and are thereupon automatically transferred to the host" (Final Office Action citing to Simionescu, Col. 21, lines 20-26).

However, the very portion relied upon by Examiner reveals Simionescu's teachings are contrary to Applicant's claimed invention. Rather than transferring data that resides in the mass storage device directly to the host system, Simionescu teaches transferring data that resides in the mass storage device to the cache. Further, rather than transferring data from the cache to the host substantially concurrently with the transfer of data from mass storage to the host, Simionescu merely teaches transferring data from the cache to the host concurrently with transferring data from mass storage to the cache. In other words, Simionescu's sectors (data) are moved from the disk drive into the cache (a first phase) and are required to wait in the cache and are not moved to the host (a second phase) until they are located during a subsequent rescanning. This is neither "directly to the host system" nor is it "substantially concurrently with the transfer of data from the cache to the host system." While Applicants acknowledge that transferring data from a mass storage device to the host may entail some level of buffering, the two-step process described by Simionescu – in which data is transferred from the host to the cache and then subsequently (in a subsequent rescanning process) transferred from the cache to the host – is a fundamentally different approach; one that does not render obvious claim 1. Claims 2 – 7 are likewise patentably distinct over the references by virtue of their respective dependence from claim 1 as well as their further respective defining limitations.

Claim 8 recites a method of retrieving data from a mass storage system, including "transferring [a] portion of the requested data from the cache memory to the host system substantially concurrently with transferring [a] portion of the requested data from the mass

storage device directly to the host system" (emphasis added). As described above, Simionescu does not teach transferring data from a mass storage device directly to the host (rather Simionescu transfers data from the mass storage device to the cache). Additionally, because Simionescu only subsequently transfers the data from the cache to the host, Simionescu fails to teach or even suggest transferring data "from the cache memory to the host system substantially concurrently with" transferring data "from the mass storage device directly to the host." Hence, claim 8, and by dependence claim 9, is patentably distinct over the cited references.

Claim 27 recites a disk memory system including logic means operable to "concurrently cause [a] disk-controller to auto-transfer [data] from [a] cache, and to cause said microprocessor to fetch [other data] directly from said disk-device." As addressed above, Simionescu merely teaches transfer of data from a disk device to cache and a subsequent transfer of data from the cache to a host. Hence, Simionescu nowhere teaches or suggests causing a microprocessor to transfer data "directly from said disk-device" as required by claim 27. Further, Simionescu nowhere teaches "concurrently" causing auto-transfer from a cache and fetching data from a disk-device. For at least these reasons, claim 27 is patentably distinct over the cited references.

Claim 28 recites a disk memory system including logic means operable to "to concurrently cause [a] disk-controller to auto-transfer [a] data-request from said cache, and to cause said microprocessor to fetch [a] data-request directly from said disk-device." As demonstrated above, Simionescu nowhere teaches or suggests causing a microprocessor to fetch data "directly from [a] disk-device" because Simionescu only teaches fetching data from the cache. Further, Simionescu nowhere teaches "concurrently" causing auto-transfer from a cache and fetching data from a disk-device. For at least these reasons, claim 28, and by dependence claims 29 – 30 are patentably distinct over the cited references.

Based on the foregoing, Applicant respectfully submits that each of the pending claims is allowable over the references of record and requests that the application be passed to issuance.

Respectfully submitted,

6/9/08

Date

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